IN THE CLAIMS

1. (Currently amended) A hardware-reconfigurable digital filter having multiple filtering modes, comprising:

logic circuitry adapted to process data corresponding to input data, the logic circuitry including ~~an X-by-Y array of~~ registers logically arrayed in an X-by-Y logical array of register for supporting at least one first filtering mode using the registers arranged ~~linearly~~ in a linear configuration which at least two rows of the logical array of registers are coupled together to form a single linear shift register and for supporting at least one second filtering mode using the registers arranged nonlinearly in a configuration different than said linear configuration, wherein each of X and Y is at least 2;

computational circuitry adapted to perform computations responsive to the logic circuitry and including at least Y multiplication logic circuits and at least Y addition logic circuits; and

mode selection circuitry adapted to switch the digital filter between the multiple filtering modes.

2. (Original) The hardware-reconfigurable digital filter of claim 1, wherein the logic circuitry and the computational circuit are configurable, in response to the mode selection circuitry, to operate in at least two of the following filtering modes: polyphase direct, polyphase transposed, finite-impulse response 11-tap, and finite-impulse response 12-tap.

3. (Original) The hardware-reconfigurable digital filter of claim 1, wherein each of the multiplication and addition logic circuits along a Y-axis direction has reconfiguration circuitry adapted to reconfigure the multiplication and addition logic circuits along the Y-axis direction the logic circuitry in response to the mode selection circuitry,

and the first filtering mode supports an impulse response filtering mode and the second filtering mode supports at one polyphase filtering mode and another impulse response filtering mode.

4. (Original) The hardware-reconfigurable digital filter of claim 1, wherein the logic circuitry and the computational circuitry are configurable to operate in one of the following filtering modes: a polyphase direct filtering mode, a polyphase transposed filtering mode, and a FIR filtering mode.

5. (Original) The hardware-reconfigurable digital filter of claim 4, wherein the mode selection circuitry adapted to switch the digital filter between the polyphase transposed filtering mode and another one of the modes.

6. (Original) The hardware-reconfigurable digital filter of claim 5, wherein the mode selection circuitry includes a first selection circuit adapted to switch the digital filter into the polyphase transposed filtering mode, and a second selection circuit adapted to switch the digital filter between modes other than the polyphase transposed filtering mode.

7. (Original) The hardware-reconfigurable digital filter of claim 6, wherein the first selection circuit is adapted to reconfigure the computational circuitry, and the second selection circuit is adapted to reconfigure the logic circuitry.

8. (Original) The hardware-reconfigurable digital filter of claim 6, wherein the modes other than the polyphase transposed filtering mode include a polyphase direct filtering mode, and two FIR filtering modes, one of the FIR filtering modes including more taps than the other of the two FIR filtering modes.

9. (Original) The hardware-reconfigurable digital filter of claim 1, wherein the logic circuitry and the computational circuit are configurable to support saving and

loading video data for context switching and switching back and forth among multiple long input lines.

10. (Original) The hardware-reconfigurable digital filter of claim 1, wherein a plurality of the registers in the array is adapted as sliced circuits along an axis defined by an alignment of the Y registers.

11. (Original) The hardware-reconfigurable digital filter of claim 1, wherein each of a first plurality of the registers in the array is adapted as a first sliced circuit along an axis defined by an alignment of the Y registers, and each of a second plurality of the registers in the array is adapted as a second sliced circuit along an axis defined by an alignment of the Y registers.

12. (Currently amended) A hardware-reconfigurable digital filter having multiple filtering modes, comprising:

logic circuitry adapted to process and mirror data corresponding to filter inputs about a data point corresponding to selected target node in a video image segment, the logic circuitry including ~~an X-by-Y array of~~ registers arrayed in an X-by-Y logical array of registers, wherein Y is greater than X and X is at least 2;

a computational circuit adapted to perform computations responsive to the logic circuitry and including at least Y multiplication logic circuits and at least Y addition logic circuit; and

mode selection circuitry adapted to direct the digital filter into a mode for performing polyphase transposed filtering ~~mode~~ by configuring the logic circuitry and the computational circuitry for processing data using the registers in a in a linear configuration which at least two rows of the logical array of registers are coupled together to form a single linear shift register ~~linear array~~ and to direct the digital filter into another filtering mode by configuring the logic circuitry and the computational circuitry for processing data using the registers in a nonlinear ~~array~~configuration different than said linear configuration.

13. (Original) The hardware-reconfigurable digital filter of claim 12, wherein a plurality of the registers in the array is adapted as sliced circuits.

14. (Original) The hardware-reconfigurable digital filter of claim 12, wherein a plurality of the registers in the array is adapted as sliced circuits along an axis defined by an alignment of the Y registers.

15. (Original) The hardware-reconfigurable digital filter of claim 12, wherein each of a first plurality of the registers in the array is adapted as a first sliced circuit along an axis defined by an alignment of the Y registers, and each of a second plurality of the registers in the array is adapted as a second sliced circuit along an axis defined by an alignment of the Y registers.

16. (Original) The hardware-reconfigurable digital filter of claim 12, wherein X is equal to two and Y is not less than 6, and wherein the multiple filtering modes include the polyphase transposed filtering mode, a polyphase direct filtering mode, and two FIR filtering modes, one of the FIR filtering modes including more taps than the other of the two FIR filtering modes.

17. (Original) The hardware-reconfigurable digital filter of claim 16, wherein one of the FIR filtering modes includes 12 taps.

18. (Currently amended) A hardware-reconfigurable digital filter having multiple filtering modes, comprising:

logic means for processing data corresponding to input data, the logic means including ~~an X-by-Y array of~~ registers logically arrayed in an X-by-Y logical array of registers for supporting at least one first filtering mode using the registers arranged in a linear configuration which at least two rows of the logical array of registers are coupled together to form a single linear shift register~~linearly~~ and for supporting at least one second filtering mode using the registers arranged ~~nonlinearly~~in a nonlinear

configuration different than said linear configuration, wherein each of X and Y is at least 2;

selection means adapted to switch the digital filter between different ones of the multiple filtering modes; and

computational means adapted to perform computations responsive to the logic means and including at least Y multiplication logic circuits and at least Y addition logic circuits.

19. (Currently amended) A hardware-reconfigurable digital filter having multiple filtering modes, comprising:

logic means for processing and mirroring data corresponding to filter inputs about a data point corresponding to selected target node in a video image segment, the logic circuitry including ~~an X-by-Y array of~~ registers logically arranged in an X-by-Y logical array of registers for supporting at least one first filtering mode using the registers arranged in a linear configuration which at least two rows of the logical array of registers are coupled together to form a single linear shift register~~linearly~~ and for supporting at least one second filtering mode using the registers arranged ~~nonlinearly~~ in a nonlinear configuration different than said linear configuration, wherein Y is greater than X and X is at least 2;

means for switching the digital filter between a polyphase transposed filtering mode and at least one other mode of the multiple filtering modes; and

means for performing computations responsive to the logic means and including at least Y multiplication logic circuits and at least Y addition logic circuits, each of the multiplication and addition logic circuits having reconfiguration means responsive to the switching means.

20. (Original) The hardware-reconfigurable digital filter of claim 19, wherein sets of the Y multiplication logic circuits and Y addition logic circuits are sliced circuits.

21. (Currently amended) A hardware-reconfigurable digital filter having multiple filtering modes, comprising:

logic circuitry adapted to process data corresponding to input data, the logic circuitry including a 2-by-6 logical array of registers for supporting a 12-tap FIR filtering mode using the registers arranged in a linear configuration which at least two rows of the logical array of registers are coupled together to form a single linear shift register~~linearly~~ and, using the registers arranged ~~nonlinearly~~in a nonlinear configuration different than said linear configuration, for supporting an 11-tap FIR filtering mode in which two of the registers at an end of the array are paired, a polyphase direct filtering mode in which each of six pairs of the registers is used to combine a single input to the pair, and polyphase transposed filtering mode in which six pairs of the registers are used to provide a wide bitwidth corresponding to a high-precision number;

computational circuitry adapted to perform computations responsive to the logic circuitry and including a multiplication logic circuit and an addition logic circuit, separately arranged, for receiving and processing data from each of the six pairs of registers; and

mode selection circuitry adapted to switch the digital filter between the multiple filtering modes.